Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Claims 1-75 are cancelled.

76. (Currently Amended) A method for making a planar semiconductor device, comprising a semiconductor substrate having a first surface and second, opposite and planar surface and a lowered effective electrical resistivity, the method comprising:

in the second, planar surface forming a highly doped drain region;

in the first surface, forming ~~an~~ one or more device active regions above the drain ~~layer~~ region, said device active regions comprising one or more wells ~~well~~ of dopants of a second and opposite polarity and in said wells one or more source regions of dopants of ~~the~~ a first polarity, the source regions laterally spaced from each other;

forming gate regions over portions of the well regions between the source regions and the drain region ~~layer~~;

~~in the second, planar surface forming a highly doped drain region;~~

in the second, planar surface of the substrate after forming the highly doped drain region, forming one or more recesses ~~resistivity-lowering bodies~~ extending from the second, planar surface of the substrate into interior portions of the semiconductor substrate, wherein said one or more recesses occur between planar regions of the second surface, forming resistivity-lowering bodies in said one or more recesses to fill the one or more recesses, the resistivity-lowering bodies comprising a material different than the semiconductor substrate and having an electrical resistivity lower than an electrical resistivity of the semiconductor substrate; and

forming a planar electrical contact layer over said second planar surface of said substrate and in electrical contact with said one or more resistivity-lowering bodies.

77. (Currently Amended) A method according to Claim ~~77~~ 76 wherein the step of forming ~~the pattern of~~ said one or more recesses comprises sawing or etching a recess into the surface of the substrate.

78. (Currently Amended) A method according to Claim ~~77~~ 76 wherein the step of forming ~~the pattern of~~ said one or more recesses comprises laser etching to form cylindrical recesses.

79. (Currently Amended) A method according to Claim 76 wherein the step of forming said one or more ~~the pattern of~~ recesses comprises forming a repeated pattern.

80. (Original) A method according to Claim 79 wherein the repeated pattern is a trapezoidal pattern.

81. (Currently Amended) A method according to Claim 76 wherein the one or more recesses comprises a grid of intersecting trenches.

Claims 82 and 83 are cancelled.

84. (Previously Presented) A method according to Claim 76 further comprising forming a barrier layer lining in at least one recess.

85. (Previously Presented) A method according to Claim 76 wherein forming the resistivity-lowering body comprises forming said body using an electrical conductor having an electrical resistivity less than about 10-4 ohm-cm.

86. (Currently Amended) A method according to Claim 76 wherein forming the one or more recesses and associated resistivity-lowering body comprises forming the one or more recesses and the associated resistivity-lowering bodies to define a proportion of the semiconductor substrate area adjacent the at least one device active region no less than 0.4 percent.

87. (Currently Amended) A method according to Claim 76 wherein forming the one or more recesses and associated resistivity-lowering body comprises forming the one or more recesses and the resistivity-lowering bodies to extend into the semiconductor substrate a distance greater than about 25 percent of a thickness of the semiconductor substrate.

88. (Currently Amended) A method according to Claim 76 wherein forming the ~~at least~~ one ~~recess~~ or more recesses and associated resistivity-lowering body comprises forming an array of recesses and associated resistivity-lowering bodies.

89. (Previously Presented) A method according to Claim 88 wherein forming the array of recesses and associated resistivity-lowering bodies comprises forming the recesses in a grid pattern.

90. (Original) A method according to Claim 89 wherein forming the grid pattern comprises cutting trenches in the second surface of the semiconductor substrate.

91. (Currently Amended) A method according to Claim 76 wherein forming the ~~at least~~ one or more device active regions ~~region~~ comprises forming at least one device region for a metal-oxide semiconductor field effect transistor (MOSFET).

92. (Currently Amended) A method according to Claim 76 wherein forming ~~the at least~~ said one or more device active regions ~~region~~ comprises forming at least one device active region for an insulated gate bipolar transistor (IGBT).

93. (Currently Amended) A method according to Claim 76 wherein forming said ~~the at least~~ one or more device active regions ~~region~~ comprises forming at least one active region of a microprocessor.

Claims 94-104 are cancelled.